

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Nobuo KARAKI

Application No.: New U.S. Patent Application

Filed: April 9, 2004

Docket No.: 119408

For: SEMICONDUCTOR INTEGRATED CIRCUIT, ELECTRONIC EQUIPMENT, AND
TRANSISTOR BACK-GATE VOLTAGE CONTROL METHOD

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

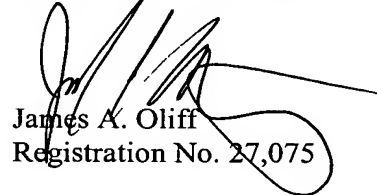
Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- ☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.
- ☒ 2. Relevance of non-English language reference No. 2 is discussed in the present specification.
- ☒ 3. An English-language Abstract of non-English language reference No. 2 is attached hereto.
- ☒ 4. A computer-generated English translation of the following Japanese Patent Publication has been obtained from the website of the Japanese Patent Office (<http://www.jpo.go.jp>), and is attached, but has not been reviewed for accuracy. See Reference 2.

- ☒ 5. A co-pending U.S. patent application is identified on Form PTO 1449 of this Information Disclosure Statement. The Examiner is respectfully requested to consider each cited application and the art cited therein during examination of the present application.

Respectfully submitted,


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